TRANSMITTAL OF APPEAL BRIEF	Docket No. M4065.0925/P925

In re Application of: Tom Teng

Application No.	Filing Date	Examiner	Group Art Unit
10/680,171-Conf. #5786	October 8, 2003	D. E. Martinez	2181

Invention: ALIGNMENT OF INSTRUCTIONS AND REPLIES ACROSS MULTIPLE DEVICES IN A CASCADED SYSTEM, USING BUFFERS OF PROGRAMMABLE DEPTHS

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: December 31, 2007 .

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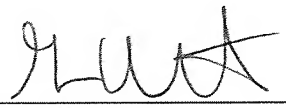

Dated: August 14, 2008

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Docket No.: M4065.0925/P925
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Tom Teng

Application No.: 10/680,171 | Confirmation No.: 5786

Filed: October 8, 2003 | Art Unit: 2181

For: ALIGNMENT OF INSTRUCTIONS AND REPLIES ACROSS MULTIPLE DEVICES IN A CASCADED SYSTEM, USING BUFFERS OF PROGRAMMABLE DEPTHS | Examiner: D. E. Martinez

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed more than two months after the Notice of Appeal filed in this case on December 31, 2007, but less than one month from the Notice of Panel Decision from Pre-Appeal Brief Review dated July 30, 2008, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.2:

I. Real Party In Interest
II Related Appeals and Interferences

III. Status of Claims
IV. Status of Amendments
V. Summary of Claimed Subject Matter
VI. Grounds of Rejection to be Reviewed on Appeal
VII. Argument
VIII. Conclusion
Appendix A Claims
Appendix B Evidence (none)
Appendix C Related Proceedings (none)

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is Micron Technology, Inc., the assignee of this application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 10 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 1-12, 18-19, and 23-62.
2. Claims withdrawn from consideration but not canceled: None.
3. Claims pending: 13-17, 20-22 and 63-64.
4. Claims allowed: None.
5. Claims rejected: 13-17, 20-22 and 63-64.

C. Claims On Appeal

The claims on appeal are claims 13-17, 20-22 and 63-64.

IV. STATUS OF AMENDMENTS

Appellant did not file an Amendment After Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

An example embodiment of the claimed subject matter is illustrated in Appellant's Figure 8, which is reproduced below.

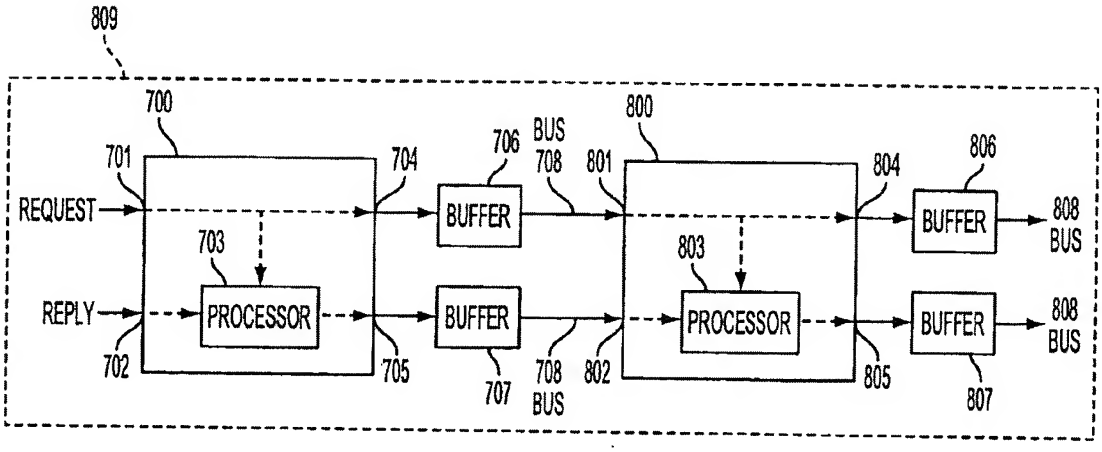

Figure 8 illustrates a semiconductor chip 809 comprising a system of cascaded devices 700, 800. According to the present application, device 700 may be any device performing a set of operations on an input signal, such as, for example, a CAM device. The device 700 receives a request signal at a first input 701 and an incoming reply signal at a second input 702. Present Application ¶ [0040]. The device 700 has first and second outputs 704, 705. Present Application ¶ [0041]. The device 700 performs a set of predetermined operations with a processor 703 and outputs an outgoing reply signal at the second output 705. The outgoing reply signal is the result of the operations performed by the processor 703 combined with the incoming reply signal at input 702. The request signal received at the first input 701 is output at the first output 704 of the device 700. *Id.*

A first buffer 706 is coupled to the first output 704 and is programmable to buffer the output request signal. Present Application ¶ [0042]. A second buffer 707 is coupled to the second output 705 and is programmable to buffer the output reply signal. *Id.* According to the present

application, the "buffers 706, 707 have programmable depths, and may be configured to be bypassed. By using buffers of programmable depths, the output request signal and/or the output reply signal may pass through the buffers 706, 707, respectively, while being delayed by the buffer for a predetermined period of time." *Id.* The amount of delay is dependant on the programmed buffer depth, which also may be programmed to bypass buffering.

After passing through respective buffers 706, 707, the buffered outputs of device 700 are sent to output bus 708 and to a downstream device 800. Present Application ¶ [0045]. The device 800 receives the request signal, buffered or not buffered, at a first input 801. *Id.* The device 800 receives the reply signal, buffered or not buffered, at a second input 802. *Id.* The device 800 functions similarly to device 700; a set of predetermined operations are performed with a processor 803 and the device 800 outputs an outgoing reply signal at a second output 805. The request signal received at the first input 801 is output at the first output 804 of the device 800. *Id.* A first buffer 806 is programmable to buffer the outputted request signal from the first output 804. A second buffer 807 is programmable to buffer the outputted reply signal from the second output 805. The buffers 806, 807 also have programmable depths, and may be configured such that bypassing of any buffer stage is allowed. *Id.*

According to the present application:

> By buffering the output signals of device 700 before passing the results down the cascade on bus 708, results for the same instruction are properly combined. In accordance with an exemplary embodiment of the invention, buffering is required in buffers 706 and 707 when device 700 and device 800 have different operational latencies. . . . Buffering is performed at a boundary between devices where the request and reply signals are not aligned. Request and reply signals are not aligned at the boundary between two adjacent devices in a cascade where the two devices have different latencies in performing their individual sets of operations. Either the request or the reply output is buffered depending on which device has a lower latency, in other words, is faster in performing its set of operations. If device 800 has a lower latency than device 700, then buffer 706 buffers the outputted request signal from output 704. If device 800 has a higher latency than device 700, then buffer 707 buffers the outputted reply signal from output 705. Typically,

> when one of the buffers 706, 707 has a programmed depth to buffer the incoming signal, the other one of the buffers bypasses at least one of its stages and may pass its signal through without buffering (if desired). This ensures that request and reply signals are aligned before outputting to a subsequent device in the cascade.
> Present Application ¶ [0046].

Turning to the claims, claim 13 recites a system of cascaded devices (e.g., devices 700, 800 illustrated on semiconductor chip 809). The claim 13 system comprises a first device (e.g., device 700) having a first input (e.g., input 701) for receiving a request signal from a first source, a second input (e.g., input 702) for receiving a first reply signal from said first source, a first output (e.g., output 704) for outputting said request signal, and a second output (e.g., output 705) for outputting a second reply signal. Present Application ¶¶ [0040]-[0041]. The claimed system further comprises a first buffer (e.g., buffer 706) having a first programmable buffer stage depth comprising a first number of buffer stages, the first buffer being coupled to said first device for receiving said outputted request signal and a second buffer (e.g., buffer 707) having a second programmable buffer stage depth comprising a second number of buffer stages, the second buffer being coupled to said first device for receiving said second reply signal. Present Application ¶¶ [0042], [0045].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The 35 U.S.C. §103(a) rejection of claims 13-17, 21-22, 63 and 64 as being unpatentable over alleged Applicant Admitted Prior Art (AAPA) in view of Smolansky.

B. The 35 U.S.C. §103(a) rejection of claim 20 as being unpatentable over the AAPA in view of Smolansky, and further in view of Jander.

VII. ARGUMENT

A. Withdrawal of the rejection of claims 13-17, 21-22, 63 and 64 as being unpatentable over alleged Applicant Admitted Prior Art (AAPA) in view of Smolansky is warranted

According to the Final Rejection, claims 13-17, 21-22 and 63-64 stand rejected under 35 U.S.C. §103(a) as being unpatentable over alleged AAPA (prior art in U.S. Publication no.

2005/0080951) in view of Smolansky (U.S. Patent no. 5,673,396). This rejection is respectfully traversed.

The Supreme Court recently held in *KSR Int'l Co. v. Teleflex Inc.* that "the [*Graham*] factors continue to define the inquiry that controls a finding of obviousness." 127 S.Ct 1727, 82 USPQ2d 1385, 1397 (2007). The *Graham* factors include determining the scope and content of the prior art, ascertaining differences between the prior art and the claims at issue, and resolving the level of ordinary skill in the pertinent art. *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966).

Appellant respectfully submits that the Final Rejection has not shown that the claims would have been obvious by conducting a full examination of the *Graham* factors. Specifically, the Final Rejection has not explicitly or implicitly resolved the level of ordinary skill in the pertinent art. "Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case." *MPEP* 2141. This is one reason why the rejection should be withdrawn.

Furthermore, claim 13 recites "a first buffer having a first programmable buffer stage depth comprising a first number of buffer stages" and "a second buffer having a second programmable buffer stage depth comprising a second number of buffer stages." The Final Rejection admits that the AAPA (i.e., the primary "reference") fails to disclose these limitations. Final Rejection at 3. The Final Rejection then states that "Smolansky teaches using buffers of programmable depth for the benefit of maximizing the use of a buffer." *Id.* The Final Rejection then makes the conclusory statement that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of AAPA and Smolansky to have the first buffer have a first programmable buffer stage depth comprising a first number of buffer stages, and the second buffer have a second programmable buffer stage depth comprising a second number of buffer stages of maximizing the use of a buffer." *Id.* Appellant respectfully disagrees with this statement as discussed in greater detail below.

In *KSR,* the Supreme Court stated that "[r]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 127 S.Ct 1727, 82 USPQ2d at 1396. As described in the Federal Register/Vol. 72, No. 195/Wednesday, October 10, 2007 Notices, page 57534, one rationale that may be used to show that a claim would be obvious is to show some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. This is the rationale that the Final Rejection provides to hold that claims 13-17, 21-22, and 63-64 are unpatentable over the AAPA and Smolansky. To reject a claim based on this rationale, the Final Rejection must articulate the following: "(1) a finding that there was some teaching, suggestion, or motivation either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; (2) a finding that there was reasonable expectation of success; and (3) whatever additional findings based on the *Graham* factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness." *Id.*

In the case at hand, the Final Rejection has failed to make a *prima facie* case for obviousness at least because the Final Rejection has failed to articulate the findings necessary to maintain a finding of obviousness under the Final Rejection's chosen rationale. Specifically, the Final Rejection has at least failed to articulate a finding that there was a reasonable expectation of success of modifying the AAPA in the manner suggested. Appellant respectfully submits that, in fact, there was no reasonable expectation of success for modifying the AAPA with Smolansky and that the alleged rationale provided in the Final Rejection (i.e., "maximizing the use of a buffer") has little to do with the claimed invention. This is another reason why the rejection of claim 13 is improper.

Moreover, presuming for the moment that the Examiner has applied the proper obviousness standard, which Appellant does not concede for at least the reasons set forth above, in order to establish a *prima facie* case of obviousness "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. §2142 (emphasis added). Appellant

respectfully submits that the AAPA and Smolansky combination fails to teach or suggest all of the limitations of independent claim 13.

For example, claim 13 recites, "a first device ...; a first buffer ... coupled to said first device for receiving said outputted request signal; and a second buffer ... coupled to said first device for receiving said second reply signal" (emphasis added). Appellant respectfully submits that the AAPA and Smolansky combination does not teach or suggest these limitations.

The Final Rejection, on the other hand, alleges that the AAPA teaches CAM devices stalling requests to teach "buffers." However, the AAPA teaches that the CAM devices are connected to each other serially, where each device D_0 ... D_n is connected only to the device in front and the device behind it in line. Therefore, the AAPA does not teach that first and second buffers are both connected to a first device. Nor does the AAPA teach that any CAM device includes a buffer to provide the stalling function. Appellant respectfully submits that the AAPA does not disclose, teach, or suggest first and second buffers connected to a first device, as recited in claim 13. Smolansky, which is cited for teaching programmable buffer stage depth, also fails to disclose, teach, or suggest these limitations. Thus, Smolansky does not remedy the deficiencies of the AAPA.

Since the alleged AAPA and Smolansky combination does not teach or suggest all of the limitations of claim 13, claim 13 and dependent claims 14-17, 21-22 and 63-64 are not obvious over the cited combination. Appellant respectfully requests that the 35 U.S.C. §103(a) rejection of claims 13-17, 21-22 and 63-64 be reversed, withdrawn and the claims allowed.

B. Withdrawal of the rejection of claim 20 as being unpatentable over the AAPA in view of Smolansky, and further in view of Jander is warranted

According to the Final Rejection, claim 20 stands rejected under 35 U.S.C. §103(a) as being unpatentable over the AAPA in view of Smolansky, and further in view of Jander (U.S. Patent no. 5,956,492). This rejection is respectfully traversed.

Claim 20 depends from claim 13. As such, claim 20 recites "a first buffer ... coupled to said first device for receiving said outputted request signal; and a second buffer ... coupled to said first device for receiving said second reply signal." As set forth above, the combination of the AAPA and Smolansky fails to disclose, teach or suggest these limitations (as well as others). The Final Rejection relies on Jander as teaching bypassing buffer stages. Jander, however, does not cure the above noted deficiencies of the AAPA and Smolansky combination. Specifically, Jander also fails to teach or suggest first and second buffers connected to a first device. Moreover, as argued previously, the Final Rejection does not follow the PTO's guidelines for rendering an obviousness rejection.

Accordingly, the rejection should be reversed, withdrawn and the claim allowed.

VIII. CONCLUSION

For the reasons given above it is respectfully submitted that the final rejection is improper. Accordingly, Appellant requests reversal of all rejections by this honorable Board..

Dated: August 14, 2008

Respectfully submitted,

By _____

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/680,171

1-12. (Canceled)

13. (Previously presented) A system of cascaded devices, comprising:

a first device having a first input for receiving a request signal from a first source, a second input for receiving a first reply signal from said first source, a first output for outputting said request signal, and a second output for outputting a second reply signal;

a first buffer having a first programmable buffer stage depth comprising a first number of buffer stages, the first buffer being coupled to said first device for receiving said outputted request signal; and

a second buffer having a second programmable buffer stage depth comprising a second number of buffer stages, the second buffer being coupled to said first device for receiving said second reply signal.

14. (Previously presented) The system of claim 13, further comprising an output bus, said output bus being coupled to said first and second buffers and to a second device.

15. (Original) The system of claim 13, wherein said second reply signal is generated from said request signal and said first reply signal.

16. (Original) The system of claim 14, wherein said first buffer buffers said outputted request signal when said second device has a lower latency than said first device.

17. (Original) The system of claim 14, wherein said second buffer buffers said second reply signal when said second device has a higher latency than said first device.

18-19. (Canceled)

20. (Previously presented) The system of claim 13, wherein:

said first buffer and said second buffer have programmable depths, and

buffer stages in said first buffer and said second buffer are bypassed.

21. (Original) The system of claim 14, wherein said first device and said second device are content addressable memory (CAM) devices.

22. (Previously presented) The system of claim 13, wherein said first and second buffers are part of a same buffer unit.

23-62. (Canceled)

63. (Previously presented) The system of claim 13, wherein the first programmable buffer stage depth is different than the second programmable buffer stage depth.

64. (Previously presented) The system of claim 13, wherein the first programmable buffer stage depth is the same as the second programmable buffer stage depth.

APPENDIX B

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

APPENDIX C

No related proceedings are referenced in II above, hence copies of decisions in related proceedings are not provided.